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Exploring the Impact of Negative Bias Temperature Instability in SiGe p-MOSFETs Utilizing a Two-Stage Model

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In recent years, Negative Bias Temperature Instability (NBTI) has emerged as a significant reliability concern for Metal-Oxide-Semiconductor (MOS) devices. NBTI leads to the accumulation of interface traps (Nit) and/or positive oxide traps (Not) in the Si/SiO_2 interface and bulk gate insulators. These defects contribute to device degradation, thereby diminishing the performance of Complementary Metal-Oxide-Semiconductor (CMOS) circuits. This project aims to investigate the characteristics of the Id/Vgs Silicon Germanium (SiGe) p-type Metal Oxide Semiconductor Field Effect Transistor (p-MOSFET) device in response to NBTI effects using two-stage model. The study delves into the impact of NBTI concerning the percentage of Germanium (Ge) concentration in the SiGe p-MOSFET device. Furthermore, the investigation explores variations in stress conditions, encompassing stress temperatures, stress and relaxation times, and stress gate voltages (Vgs). The research utilized Silvaco Technology Computer Aided Design (TCAD) TOOLS, employing Athena as a process simulator and Atlas as a device simulator. The simulation results reveal a discernible trend of increasing degradation in terms of drain current (Id) and threshold voltage (Vth) shift as the percentage of Ge, stress temperature, stress voltage, and stress time are elevated. This suggests that optimizing the percentage of Ge has the potential to ameliorate the reliability effects of NBTI.

Keywords: NBTI; SiGe p-MOSFET; Ge; instability; Vth; temperature; Id-Vgs; two-stage model

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In 1965, Gordon Moore observed that the transistor counts on a chip experienced exponential growth over time, a phenomenon now known as Moore's Law. The ability of Moore's Law to hold true is attributed to the exponential decrease in transistor size. At the time of Moore's prediction, in 1965, the transistor size was 100 nm. Over the past three decades, transistor size has exponentially decreased from micrometers to sub-micrometers to deep sub-micrometers, validating Moore's prediction [1]. In contemporary Complementary Metal-Oxide-Semiconductor (CMOS) technologies, Negative Bias Temperature Instability (NBTI) has emerged as a critical reliability concern at both the device and circuit levels. During NBTI testing of PMOS devices under negative gate stress at high temperatures, a change in threshold voltage (Vth) is observed [2]. This shift, known as bias temperature instability, is considered a failure when it exceeds a predetermined threshold, typically 30 mV. Despite achieving well-behaving CMOS devices with aggressively scaled Equivalent Oxide Thickness (EOT) down to 0.5 nm, ensuring a ten-year lifetime for expected operating voltages remains uncertain due to the increasing interfacial oxide electric field (Eox) of NBTI. This reliability challenge poses a potential obstacle [3]. Therefore, to enhance CMOS performance, the incorporation of high-mobility channels, such as Silicon Germanium (SiGe) p-MOSFET and Ge, is being explored. SiGe p-MOSFET is deposited on the Silicon (Si) substrate to increase carrier mobility and, consequently, improve drive current. The strained Si technology introduces an alloy layer combining Si and Germanium (Ge) to enhance carrier mobility and transistor speed. Meanwhile, a strained Si channel induces tensile stress through the elastic relaxation of a buried compressive SiGe layer. Accordingly, this technology increases semiconductor mobility and improves depressions at the source and drain, allowing for a higher increase in saturation drive current [4].

Recent research [5], introduced the two-stage model to accurately describe the NBTI degradation mechanism over various time scales. The model

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comprises recoverable degradation, involving hole trapping in oxygen vacancies, and permanent degradation, where Pb centers are created through hydrogen capture. Furthermore, the multi-phonon-field-aided hole trapping mechanism proposed by [6] suggested that the creation of E centers from oxygen vacancy precursors contributes to the de-passivation of interface states. This, in turn, couples the created oxide and interface state components. Moreover, previous work [7] asserted that Ge-based technology holds promise for increased NBTI robustness. Optimization of the SiGe p-MOSFET gate stack, including a high Ge fraction (55%) in the channel, demonstrated enhanced reliability. This improvement was transferable to various device structures, including pure Ge channel p-MOSFETs. Further experimental findings in [7] explained the relationship between the Ge fraction and quantum well thickness. Hence, maximizing the valence band offset between SiGe and Si, along with a higher Ge fraction and a thick quantum well, helps reduce the fraction of accessible defects and enhances NBTI robustness.

In this work, the two-stage model will be implemented to analyses the NBTI degradation in SiGe p-MOSFET devices. By implementing the two-stage model the permanent and recoverable component will be considered in this simulation study. We demonstrate the degradation level of the SiGe p-MOSFET by looking at different stress temperature, stress and relax time as well as the Ge contents on the NBTI parameter under study.

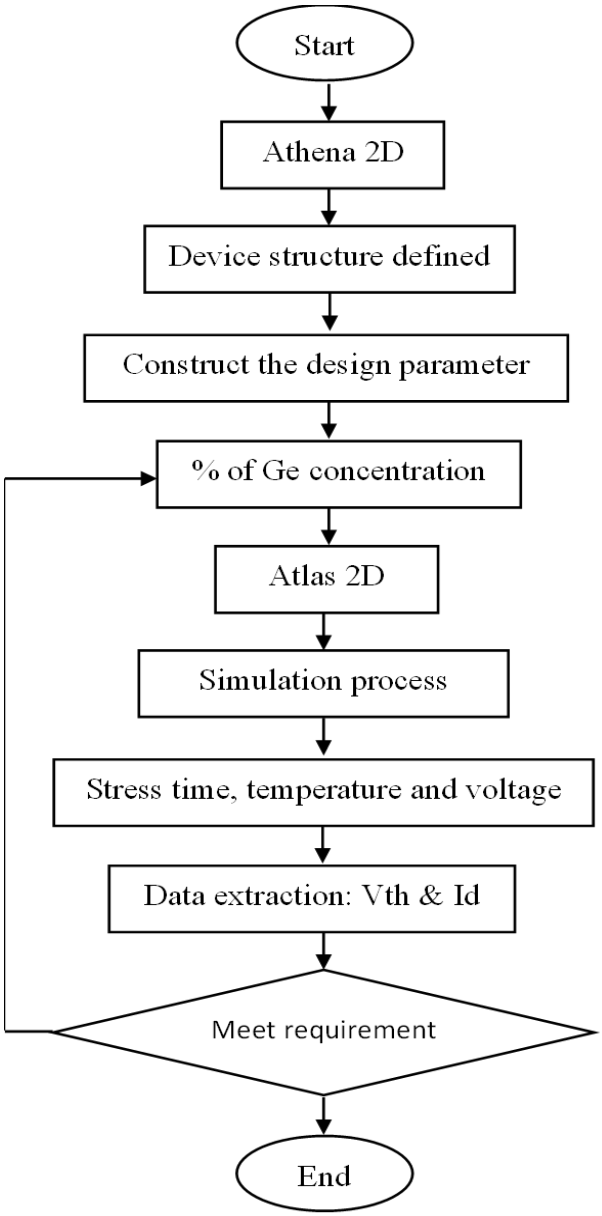

Figure 1. The flowchart of device modelling using Silvaco TCAD.

METHODOLOGY

Overall Simulation Framework

The flowchart presented in Figure 1 outlines the process for modeling the SiGe p-MOSFET and determining two-stage NBTI parameters using Silvaco TCAD tools. Initially, in Athena 2D, the fabrication of the SiGe p-MOSFET device structure is defined, and the subsequent construction of design parameters is performed. The simulation employs SiGe for device modeling. The operational design is simulated by varying the percentage of Ge concentration to examine the impact of SiGe p-MOSFET on NBTI. Following the fabrication steps, Atlas 2D initiates the simulation of stress time, stress temperature, and stress voltage to explore the NBTI effect using the two-stage model. In addition, post-simulation, pertinent data, such as threshold voltage (Vth) and the Id characteristic, is extracted for analysis. The process concludes when the observed results meet the specified requirements. All design parameters serve as inputs when building the deck of the Silvaco ATLAS tools.

SiGe p-MOSFET Fabrication Process

Figure 2 illustrates the flowchart detailing the fabrication process of the SiGe p-MOSFET. This process is geared towards generating the SiGe p-MOSFET with NBTI. Initially, the substrate material is selected, and an initial grid is established, specifying the coordinates (x, y) and the spacing for each x and y line. The impact of selective epitaxy is achieved by depositing layers with thicknesses of 2.5 μm and 0.5 μm, followed by etching the oxide thickness. Consequently, the top oxide is eliminated as a result of the etching process. The epitaxy process involves the growth of a crystalline film with the proper orientation on a substrate. A notable advantage of pursuing this condition is that it compels the crystal to expose free surfaces not naturally obtained through cleavage or typical bulk growth [8].

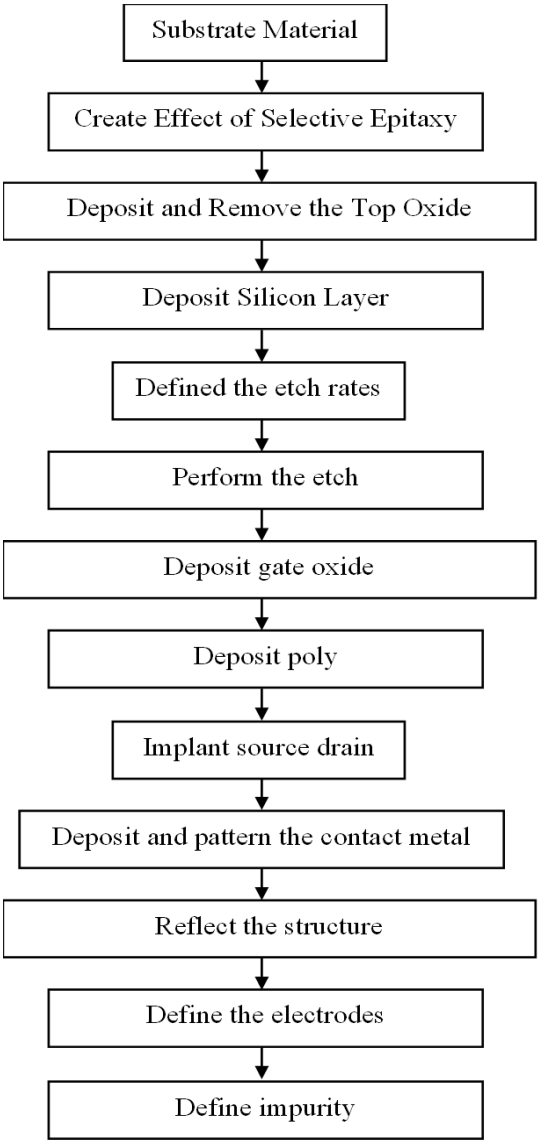

Figure 2. The flowchart of the SiGe p-MOSFET fabrication.

Following the removal of the top oxide, a Si layer is deposited with a thickness of 0.025 μm, and the Ge mole fraction is set at 0.35. Boron serves as the P-type dopant in the SiGe p-MOSFET, while Phosphorous acts as a donor. Additionally, the etch rates for Si, oxide, and SiGe p-MOSFET have been defined, employing isotropic etching for the etch process. Once all materials have undergone etching, a gate oxide is deposited with a thickness of 0.016 μm. Subsequently, a polysilicon layer with a thickness of 0.2 μm is deposited at the gate. After patterning the gate, the source and drain are subjected to implantation with Borophosphosilicate glass (BPSG). Flow-type Chemical Vapor Deposition (CVD) reactors are utilized to deposit BPSG thin films, featuring varying boron and phosphorus contents. The film formation is facilitated through chemical oxidation processes. Films can be synthesized using diverse compounds containing Si, boron, and phosphorus [9]. Moreover, the contact metal has been both deposited and patterned, and the structure has been mirrored to the right. Additionally, electrodes have been specified for the left source, right drain, and gate positioned between the source and drain with the lines x = 2.5 and 3.1. Lastly, the impurity, acting as an acceptor or donor in the SiGe p-MOSFET material, has been defined.

The schematic diagram of the SiGe p-MOSFET, utilized for the modeling and simulation in this project, is presented in Figure 3, while the simulated device is depicted in Figure 4.

NBTI Model

NBTI poses a notable challenge to the reliability of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). Since that p-channel MOS devices typically function with a negative gate-to-source voltage, this issue becomes particularly acute. The instability associated with NBTI has been a concern for MOSFETs since as early as 1996 [10]. The scaling of technology, elevated chip operating temperatures, the substitution of buried channel devices with surface p-channel MOSFETs, and the regular introduction of nitrogen into thermally grown SiO_2 have collectively transformed it into a reliability concern in Si integrated circuits [11].

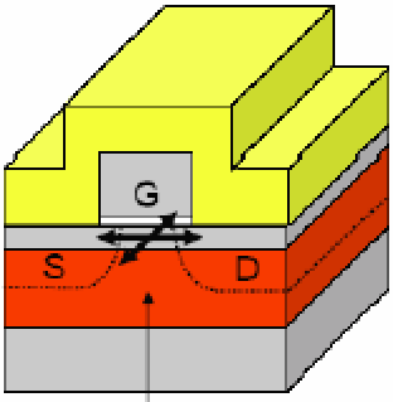

Figure 3. The schematic diagram of SiGe p-MOSFET.

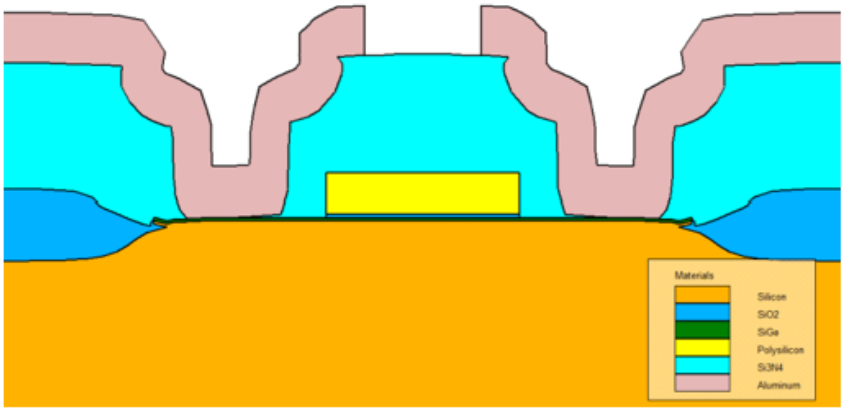

Figure 4. Structure of the SiGe p-MOSFET.

It is widely recognized that NBTI degrades p-MOSFET transistors during circuit operation, particularly when a p-MOSFET transistor is in the conducting state. Therefore, a thorough analysis of NBTI degradation necessitates logic state examination. The density of interface traps (Nit) at the drain can be reduced, and the Vth shift will be less pronounced when a Source/Drain (S/D) bias is applied. Given that the drain current (Id) exhibits a linear correlation with Vds, it can be expressed as:

$$I_d = \frac{W}{L}\mu C(V_{gs} - V_{th})V_{ds} \quad (1)$$

Here, *w* represents the channel length in centimeters (cm), *C* is the oxide capacitance in Farads per square centimeter (F/cm²), and *u* denotes the carrier mobility in square centimeters per volt-second (cm²/(V-sec)). The calculation of NBTI degradation during stress is determined as follows [12]:

$$\Delta N_{IT} = \frac{q}{C_{ox}} x(\Delta N_{IT} + \Delta N_{HT} + \Delta N_{OT}), \quad (2)$$

Where ΔN_{IT} represents the generation of interface traps, ΔN_{HT} corresponds to hole trapping in pre-existing defects, and ΔN_{OT} signifies the generation of oxide bulk traps, the

$$\Delta V_T = \Delta V_{IT1} + \Delta V_{IT2} + \Delta V_{HT}. \quad (3)$$

Broadly, the complete recovery encompasses three distinct components: 1) fast recovery of ΔV_{HT} and ΔV_{OT}; 2) rapid electron capture by a portion of ΔV_{IT} (ΔV_{IT1}); and 3) gradual recovery of the residual ΔV_{IT} (ΔV_{IT2}). During the NBTI recovery phase, the trapping of holes in N_{HT} and N_{OT} can rapidly recuperate within a few seconds. Moreover, below the Fermi level, the fracture in N_{IT} may promptly capture electrons, contributing to a quick recovery.

The two-stage NBTI model can elucidate negative bias temperature instability, encompassing the formation of E' centers from their neutral oxygen vacancy precursors. These centers demonstrate the capacity for repeated charging and discharging before complete annealing, delineating the initial stage of degradation [13]. During the second stage, a positively charged E' center has the potential to initiate the de-passivation of Pb centers at the Si/SiO_2 interface or KN centers in oxynitrides, leading to the formation of an unpassivated silicon dangling bond. This model offers insights into degradation and recovery across diverse bias voltages and stress temperatures. It accounts for the observed asymmetry between stress and recovery, as well as the pronounced sensitivity to bias and temperature during the recovery process. Remarkable consistency with data from three markedly distinct technologies (thick SiO2, SiON, and HK) has been achieved, bolstering the notion that NBTI is influenced by the chemistry of the amorphous SiO_2/Si interface region [6].

Device & Simulation Conditions

Various parameters have been explored and studied to comprehend the impact of SiGe p-MOSFET on NBTI using a two-stage model. These parameters include the Ge mole fraction, stress temperature, stress time, and gate voltage (Vg). In the simulation, the Ge mole fraction was varied while keeping other factors constant. Subsequently, the Id was scrutinized by altering the stress temperature while maintaining a constant stress time. Additionally, the Vth was investigated by varying the gate voltage (Vg). Finally, the stress time was varied to examine the NBTI effects on the drain current while maintaining a constant stress temperature. Table I and Table II summarized the varied and fixed parameters used in the simulation.

Table 1. Varied Parameters.

Parameters	Values	Reference
% Of Ge Concentration	35%, 45%, 55%	[14], [15]
Stress Temperature	373 K, 393 K, 400 K, 420 K	[5], [6]
Stress Time	0.1 s, 1 s, 10 s, 100 s	[16], [5]

Table 2. Fixed Parameters.

Parameters	Values
% Of Ge Concentration	35%
Si cap	0.025 μm
Stress Temperature	393K
Stress time	100 s
Relaxed time	1000 s
Voltage gate	-1.75V

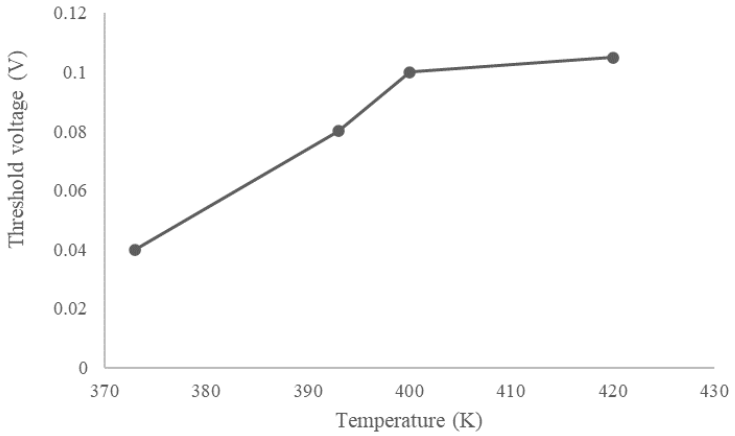

Figure 5. Threshold voltage shift with different temperatures.

RESULTS AND DISCUSSION

In this segment, we have explored the impact of parameters such as the percentage of Ge concentration, temperature, stress, and relaxation time on the performance of the SiGe p-MOSFET device concerning NBTI, employing a two-stage model. The analysis includes the extraction of Vth and Id characteristics to assess the effects of NBTI.

Effect of NBTI on Different Temperatures

To examine the influence of temperature variations on NBTI in the SiGe pMOSFET device, alterations in Vth and Id were monitored. In Figure 5, the stress temperature was manipulated while maintaining a constant Vg of -1.75. An increase in temperature, there is a corresponding increase in the Vth. This phenomenon can be attributed to the fact that as the energy of holes escalates, the trapping rate also rises [5][17]. Moreover, with the ascent in temperatures, the Si bonds at the interface become more susceptible to breakage, leading to an augmentation in the number of interface traps. When a bias is applied to the gate, a reaction related to the electric field will occur at the interface, and the passivated Si-H bonds will be broken, resulting in interface traps. Higher negative gate biased applied lead to more degradation. Meanwhile, the high stress voltage and high temperature will weaken the existing Si-H bonds, so it will also aggravate NBTI [18][19][20][21].

Effect of NBTI on Different Stress Conditions

The Id is likewise influenced by the Vth, manifesting a twofold degradation in saturation, as observed in the results [22]:

$$I_{Dsat} \approx \frac{w\mu_{eff}C_{ox}}{2L}(V_G - V_T)^2 \rightarrow \frac{1}{I_D}\frac{dI_D}{dV_T} = \frac{2\Delta V_T}{V_G - V_T} \quad (4)$$

The investigation of the Id aims to explore the impact of NBTI under various stress conditions. This involves varying stress times while maintaining a constant Vg of -1.75V and a temperature of 393K. The stress times considered were 0.1ms, 1ms, 10ms, and 100ms. The outcomes depicted in Figure 6, indicate that as the stress time increases, there is a potential decrease in the Id.

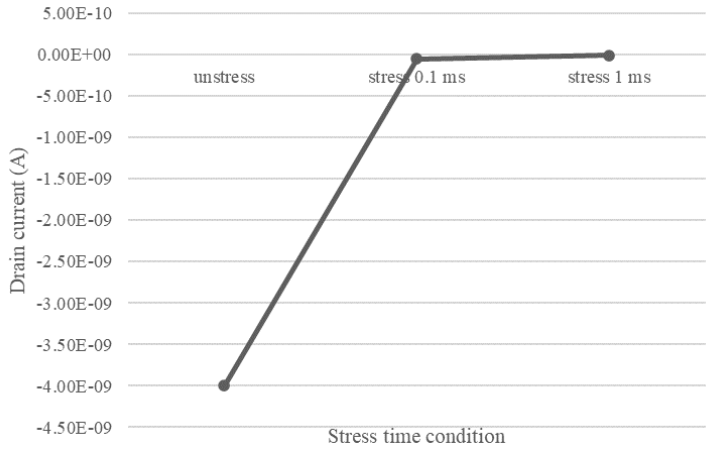

Figure 6. Drain current when stress applied.

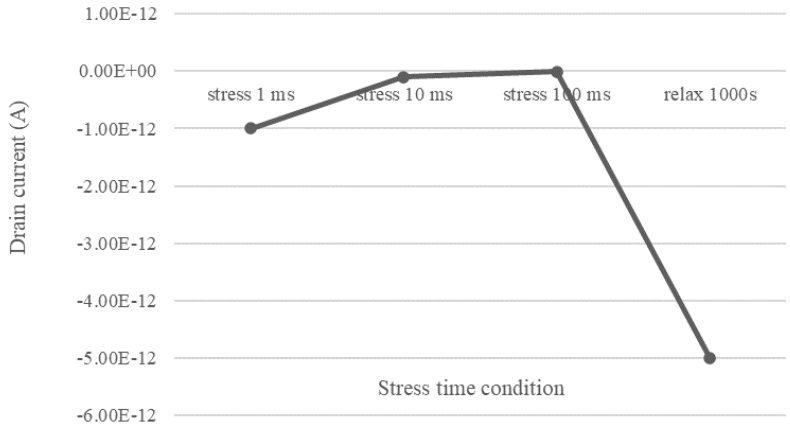

Figure 7. Drain current when stress and relaxation are applied.

In the stress phase of the device's operation, characterized by a high negative gate bias and elevated temperature, the entrapment of holes in the oxide occurs, reducing the device's performance. This phenomenon is attributed to holes being captured in oxygen vacancy precursors under stress, potentially resulting in the formation of E' centers near the interface. Figure 7 illustrates the impact of NBTI after a relaxation period of 1000 seconds. It is well-established that the recovery process takes considerably longer than the duration for degradation to accumulate [6]. A smaller fraction of defects become apparent during recovery, mainly since the Fermi-level shifts toward the mid-gap. The drain current degradation decreases after 1000 s relax which explains the recoverable of component degradation [23], [24].

Effect of NBTI on Different Process Variations

The optimization of NBTI reliability was explored by considering different percentages of Ge concentration in Si as it is well known that Ge-based technology holds the promise of significantly enhancing NBTI robustness [25][26]. As depicted in Figure 8, introducing Ge into the channel significantly enhanced NBTI reliability. An increase in the Ge mole fraction to 55% resulted in a higher Vth, while maintaining a constant Si thickness of 0.025 μm and oxide thickness of 0.05 μm. Similar observations found in [27] which state that a higher Ge fraction correlates with a more positive Vth_0. This trend can be attributed to the reduction in channel bandgap, which is anticipated to vary depending on the Ge fraction, as follows:

$$E_G(Si_{1-x}Ge_x \approx E_G(Si) - 0.74x) \quad (5)$$

This figure illustrates the influence of changing the Ge mole fraction on the Vth. Holes are confined to the valence band of the strained SiGe p-MOSFET due to the increasing valence band offset with higher Ge content. Consequently, the Vth variation for different SiGe p-MOSFET structures with Ge contents of 35%, 45%, and 55%, and constant strained SiGe layer thickness, indicates that an increased Ge mole fraction shifts the Vth towards the valence band offset, particularly for a sufficiently thick SiGe layer.

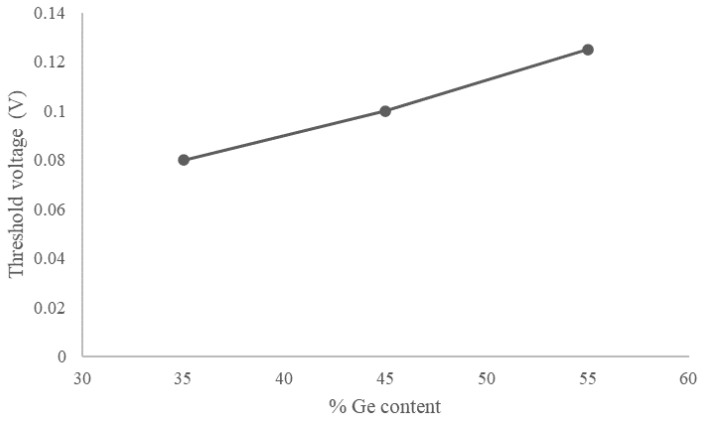

Figure 8. Threshold voltage shift based on different % Ge concentrations on SiGe.

This is attributed to the narrower bandgap and higher intrinsic carriers, leading to a decrease in $|V_T|$ as Ge concentration increases. According to a study [28], it is likely that the increased negative fixed charge with higher Ge concentrations causes the flat band voltage (V_{FB}) to shift positively.

CONCLUSION

This study provides a comprehensive analysis of simulation outcomes for the SiGe p-MOSFET structure under various stress conditions, utilizing a two-stage model. According to the findings, changes in the device's performance, as observed through parameters such as Id characteristic and Vth, are significantly influenced by alterations in temperature, stress Vg, stress conditions, stress and relaxation time, and the percentage of Ge concentration. The results highlight that a higher Ge fraction correlates increased the Vth_0. The investigation into NBTI effects at different temperatures reveals an increase in Vth due to higher temperatures during pre-stress, resulting in greater occupation during the initial stress period. It is demonstrated that the occupation further increases with prolonged stress times and is more pronounced at elevated temperatures. Ultimately, the simulation indicates that a lengthier stress decreases the Id affected by NBTI.

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